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SEQUENTIALLY PROCESSED CIRCUITRY

TECHNICAL FIELD

The invention concerns sequentially processed circuitry.

BACKGROUND

Traditionally printed circuit boards have been manufactured by one of two basic techniques. The first technique begins with a copper (or other conductive material) coated substrate and selectively removes the conductive material in accordance with a photo defined masking and etching process defined pattern and chemical etch. The second basic method utilizes the addition of conductive material by way of photodefined patterns to provide properly interconnected conductors. In the construction of a sequentially processed multilayer printed wiring board, as opposed to a laminated multilayer board, each dielectric/conductor layer is applied by a sequence of processes which construct, first, the dielectric, then the vias or interlayer interconnection, then the conductors. Such processes use a combination of addition and etching of metals as well as addition and removal of applied dielectric to obtain both the conductors and the dielectric with conductive holes (vias) which connect conductors on one layer with conductors above and below.

These processes and a further development of these processes are described in US 5,260,170. However it can be considered a disadvantage to use these processes as the most sensitive circuitry is left unprotected on top, i.e. there is a need for a method of manufacturing a sequentially processed circuit which does not leave sensitive circuitry unprotected.

SUMMARY

An object of the invention is to define a sequentially processed circuit which does not leave sensitive circuitry unprotected and also to define a method of manufacturing the same.

Another object of the invention is to define an encapsulation of sequentially processed circuitry of extremely thin layers of environmentally less resistant materials, such as less stable polymers, for example dielectric of thin layers of acrylate.

A further object of the invention is to define a sequentially processed circuit with improved cooling of the circuit.

The aforementioned objects are achieved according to the invention by an encapsulated circuit comprising a thin interface layer with possibly one or more vias for input/output interface to the circuit. The encapsulated circuit further comprises one or more sequentially processed circuit layers added to one side of the interface layer. The sequentially processed circuit layers are preferably made by additive offset printing technology. The encapsulated circuit further comprises a layer of adhesive. A first side of the adhesive layer is attached on top of the uppermost and most exposed circuit layer. The encapsulated circuit further comprises a support carrier attached on a second side of the adhesive layer.

The aforementioned objects are also achieved according to the invention by a process for the formation of an encapsulated circuit having at least one layer of circuitry. The encapsulated circuit has a first side as an interface side and a second side as a protective cover. According to the invention the process comprises a plurality of steps. In a first step applying at least one layer of sequentially processed circuitry on a first side of an interface carrier, a second side of the interface carrier being the interface side of the encapsulated circuit. In a second step joining the last applied sequentially

processed circuitry layer to a support carrier by means of an adhesive layer, the support carrier forming the protective cover of the second side of the encapsulated circuit.

The process preferably either further comprises the step of applying the adhesive layer on top of the last applied sequentially processed circuitry layer, or the step of applying the adhesive layer to the support carrier.

Preferably the application of at least one of the at least one sequentially processed circuitry layer is by means of offset printing technology. Suitably a dielectric of at least one of the at least one sequentially processed circuitry layer is acrylate. Additionally, the application of the adhesive layer is preferably by means of offset printing technology.

The support carrier can in some embodiments be at least a part of a cover housing in which the encapsulated circuit is mounted. In some embodiments the support carrier is at least a part of an enclosure on which the encapsulated circuit is mounted. In some embodiments the support carrier is rigid, in other embodiments the support carrier is bendable.

Preferably at least one of the at least one sequentially processed layer comprises connection circuitry. In some embodiments at least one of the at least one sequentially processed layer comprises at least one passive component. In some embodiments at least one of the at least one sequentially processed layer comprises at least one active component.

Advantageously the interface carrier comprises at least one via, the at least one of the at least one via is preferably solid. In some embodiments the interface carrier is bendable. The interface carrier is preferably made of polymide or polyester.

The aforementioned objects are also achieved according to the invention by an encapsulated circuit having at least one layer of circuitry. The encapsulated circuit has a first side as an interface side and a second side as a protective cover. According to the invention the circuit comprises a plurality of layers. The circuit comprises an interface layer having a first side and a second side, the first side of the interface layer being the interface side of the encapsulated circuit. The circuit further comprises at least one layer of sequentially processed circuitry on the second side of the interface layer. The circuit also comprises a support layer forming the protective cover of the second side of the encapsulated circuit. Finally the circuit also comprises an adhesive layer between a top of the last sequentially processed circuitry layer and the support carrier.

Advantageously at least one of the at least one sequentially processed circuitry layer has been added by means of offset printing technology and suitably a dielectric of at least one of the at least one sequentially processed circuitry layer is acrylate. In some embodiments the adhesive layer has preferably been added by means of offset printing technology.

The support layer can is some embodiments be at least a part of a cover housing in which the encapsulated circuit is mounted. In some embodiments the support carrier is at least a part of an enclosure on which the encapsulated circuit is mounted. In some embodiments the support layer is rigid in other embodiments the support layer is bendable.

Advantageously at least one of the at least one sequentially processed layer comprises connection circuitry. In some embodiments at least one of the at least one sequentially processed layer comprises at least one passive component. In some embodiments at least one of the at least one sequentially processed layer comprises at least one active component.

The interface layer preferably comprises at least one via and preferably at least one of the at least one via is solid. In some embodiments the interface layer is bendable and preferably made of polymide or polyester.

The aforementioned objects are also achieved according to the invention by a device comprising wireless communication means, which device comprises an encapsulated circuit according to any above described encapsulated circuits according to the invention or encapsulated circuit according to any above described process according to the invention.

The aforementioned objects are also achieved according to the invention by a wireless or wireless mobile terminal which comprises an encapsulated circuit according to any above described encapsulated circuit according to the invention for wireless communication.

By providing an encapsulated circuit according to the invention a plurality of advantages over prior art circuit boards are obtained. Primary purposes of the invention are to provide a well protected and well cooled circuit by cheap manufacturing methods. Other advantages of this invention will become apparent from the detailed description.

Brief description of the drawings

The invention will now be described in more detail for explanatory, and in no sense limiting, purposes, with reference to the following figures, in which

Fig. 1a-1e shows a cross section of sequentially processed circuitry according to the invention during different processing steps.

Detailed description

Encapsulation of printed circuits, with or without active and/or passive cuircuitry, that are processed sequentially is necessary to prevent destruction of the

circuits, especially if they are made of environmentally sensitive materials and/or with very thin layers. There is a desire to reduce conductors of a cuircuit board to less than 5 μm thick and less than 20 μm wide. This has raised an interest in using less stable polymers such as acrylat as thin layers of dielectric. It has been proposed to use offset printing for manufacturing printed circuits and also for manufacture of active and passive components, such as transistor functions, resistors, capacitors, sensors, and emitters, with the same process by means of conductive polymers. The process used is of an additive type. Using offset printing technology will enable manufacturing of surfaces in the order of 450 mm by 600 mm for a multiple of products with sizes in the range of approximately 100 mm by 150 mm to 10 mm by 10 mm. The finished products are unfortunately extremely sensitve to external physical contact. According to the invention, sequentially processed layers are built on an interface carrier. Thereafter a layer of adhesive is added to cover the sequentially processed layers and then a support carrier is stuck onto the adhesive. Alternatively a layer of adhesive is added to a support carrier after which the interface carrier is stuck to the support carrier with the sequentially processed layers closest to the adhesive on the support carrier. A sandwich construction is thus attained with the interface carrier on one side and the support carrier on the other side protecting the fragile layers within.

As an example, a temperature log of a frozen merchandize is desired. An appropriate circuit is manufactured on an interface carrier of at least semi-transparent polyester. The circuit side is joined by an adhesive with a cardboard box in which the frozen merchandize is to be transported. The cardboard box of the frozen merchanize will then function as the support carrier. The circuit with appropriate sensors is mounted directly onto the object to be monitored and a readout of conditions can be made through the interface carrier by means of light emitting diodes. The adhesive layer between the carboard box, the support carrier, and the circuit can be shaped such that sensors or electrical contacts are not covered but have a direct contact with the support carrier, while at the same time providing a sufficient seal.

In order to clarify the method and device according to the invention, some examples of its use will now be described in connection with Figures 1a to 1e. Figures 1a to 1e shows a cross section of sequentially processed circuitry according to the invention during different processing steps.

In a first step, as is shown in Figure 1a, the manufacturing starts with an interface carrier 100. The interface carrier 100 is preferably made of a flexible or semi-flexible material such as polymide or polyester, suitably in the range of 25 μm thick. In some embodiments the interface layer, only or in addition, provides an optical interface to underlying sequentially processed circuitry by being at least semi transparent. The underlying sequentially processed circuitry might comprise light emitting diodes that are used for a visual readout on a first side 101 of the interface layer. The first side 101 of the interface layer can also be arranged for possible external electrical connections to suitable parts of the sequentially processed circuitry by means of optional via holes 102 such as micro vias and other suitable circuitry such as copper conductors up to approximately 35 μm thick. The optional via holes 102 provide for electrical interconnections between the first side 101 and a second side 109 of the interface carrier 100. The vias 102 are preferably solid vias to provide cooling of sequentially processed circuitry on the second side 109. The vias 102 and any other electrical circuitry are preferably preprocessed. The second side 109 of the interface carrier 100 is the manufacturing support for the sequentially processed circuitry and will also provide any possible electrical connections to it. Preferably an area of the interface carrier 100 is larger than any area of a sequentially processed layer.

In a second step, as is shown in Figure 1b, a first sequential circuitry layer 110 is manufactured onto the second side 109 of the interface carrier 100. The circuitry layers are suitably added by offset printing technology. The

layers are either just electrical interconnection circuitry, passive or active components. Figure 1c shows a second sequential layer 120 being added. A printed circuit according to the invention comprises at least one circuitry layer 110, preferably at least two layers 110, 120. The process of adding sequential layers is repeated as many times as desired. When all the layers 110, 120 have been added to the second side 109 of the interface carrier 100, then, as shown in Figure 1d, an adhesive layer 190 is added on top of the last added circuitry layer, in this example the second layer 120. The adhesive layer 190 is preferably also applied with offset printing techniques. The adhesive layer 190 will seal the sequentially processed layers 110, 120. The adhesive layer 190 may suitably be fluid epoxy added by roller coating. In some embodiments according to the invention the adhesive layer is first added to a support carrier. The adhesive layer 190 may be formed such that it only covers the sequential layers 110, 120, or extends beyond the sequential layers 110, 120, i.e. an area of the adhesive layer 190 is larger than an area of the largest sequential layer. The adhesive layer can preferably be of substantially a same area as the interface carrier 100, but in some embodiments it can be larger and in other embodiments it will be smaller. The adhesive layer 190 will preferably seal the sequential layers 110, 120. In some embodiments the adhesive layer 190 may comprise apertures for, for example, connections, electrical or other, to a support carrier.

In a final step, as shown in Figure 1e, a support carrier 199 is stuck onto the adhesive layer 190. Or alternatively a carrier with an adhesive layer is stuck onto the sequentially processed layers. The support carrier 199 will typically be in the order of millimeters to approximately 200 μm thick. The main purpose of the support carrier 199 is to provide a physical barrier and protection to the sensitive sequentially processed layers 110, 120. The support carrier 199 can, for example, be of paper, plastic or metal, be bendable or rigid, be a part of a chassi or cover/case/housing of an apparatus in which the circuitry is mounted, or be a carrier/box onto which

the circuitry is mounted. As an example the casing might be of a mobil phone or an accessory to it, such as blue tooth, in which case the electronic circuitry, with or without active or passive components, will take very little space and still be very well protected. If the support carrier 199 is a part of a casing, then most likely it will not be plane. The support carrier 190 may also comprise apertures, then preferably aligned with any apertures in the adhesive layer 190, for electrical access or access to any sensor on the outermost sequential layer 120.

The basic principle of the invention is to manufacture a plurality of extremely thin and vunerable sequentially processed circuitry layers on an interface carrier, turn the whole thing over and join an uppermost and most exposed circuit layer with a support carrier by means of a layer of adhesive that is either added to the uppermost circuit layer or the support carrier. The interface carrier, onto which the circuit layers have been added, will provide a communication interface to the circuitry.

The invention is not restricted to the above described embodiments, but may be varied within the scope of the following claims.

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FIGURE 1

100	an interface carrier,
101	a first side of the interface carrier for external connections,
102	via holes such as micro vias for electrical interconnections between the first and a second side of the interface carrier,
109	the second side of the interface carrier for circuit layers and connections to these,
110	a first sequential layer,
120	a second sequential layer,
190	an adhesive layer,
199	a support carrier.